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NON-PROVISIONAL APPLICATION FOR U. S. PATENT UNDER 37 CFR 1.53(b)  
TRANSMITTAL FORM

Attorney Docket No. TI-28098

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Inventor(s): Donald C. Abbott  
Paul R. Moehle

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09/525105  
03/14/00

For: **GOLD SPOT PLATED LEADFRAMES FOR SEMICONDUCTOR  
DEVICES AND METHOD OF FABRICATION**

Enclosed are:

- 2 Sheets of formal drawings and 23 pages of Specification (including Abstract)  
x A Declaration/Power of Attorney  
x Assignment with form PTO 1595

Please amend the specification by inserting before the first line the sentence:

This application claims priority under 35 USC § 119 based upon **Provisional Patent  
Application number 60/125,304, filed 03/19/99.**

FEE CALCULATION					FEE
	NUMBER		NUMBER EXTRA	RATE	BASIC FEE \$ 690.00
Total Claims	22	-20 =	2	X \$22 =	\$44.00
Independent Claims	6	- 3 =	3	X \$82 =	\$246.00
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March 13, 2000

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Assistant Commissioner for Patents  
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Re: Patent Application For:  
**GOLD SPOT PLATED LEADFRAMES FOR SEMICONDUCTOR  
DEVICES AND METHOD OF FABRICATION**  
Attorney Docket No. TI-28098  
Our File: 1000-2107

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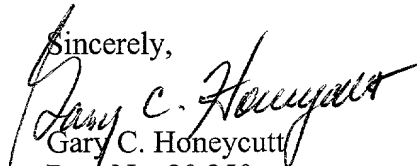
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004 FEB 29 2000

GOLD SPOT PLATED LEADFRAMES  
FOR SEMICONDUCTOR DEVICES AND METHOD OF FABRICATION

FIELD OF THE INVENTION

5           The present invention is related in general to the field of semiconductor devices and processes and more specifically to the materials and fabrication of leadframes for integrated circuit devices.

10   DESCRIPTION OF THE RELATED ART

          The leadframe for semiconductor devices was invented (US Patents # 3,716,764 and # 4,034,027) to serve several needs of semiconductor devices and their operation  
15 simultaneously: First of all, the leadframe provides a stable support pad for firmly positioning the semiconductor chip, usually an integrated circuit (IC) chip. Since the leadframe including the pads is made of electrically conductive material, the pad may be biased, when needed, to  
20 any electrical potential required by the network involving the semiconductor device, especially the ground potential.

          Secondly, the leadframe offers a plurality of conductive segments to bring various electrical conductors into close proximity of the chip. The remaining gap between  
25 the ("inner") tip of the segments and the conductor pads on the IC surface are typically bridged by thin metallic wires, individually bonded to the IC contact pads and the leadframe segments. Obviously, the technique of wire bonding implies that reliable welds can be formed at the (inner) segment  
30 tips.

Thirdly, the ends of the lead segment remote from the IC chip ("outer" tips) need to be electrically and mechanically connected to "other parts" or the "outside world", for instance to assembly printed circuit boards. In the overwhelming majority of electronic applications, this attachment is performed by soldering. Obviously, the technique of soldering implies that reliable wetting and solder contact can be performed at the (outer) segment tips.

It has been common practice to manufacture single piece leadframes from thin (about 120 to 250  $\mu\text{m}$ ) sheets of metal. For reasons of easy manufacturing, the commonly selected starting metals are copper, copper alloys, iron-nickel alloys for instance the so-called "Alloy 42"), and invar. The desired shape of the leadframe is etched or stamped from the original sheet. In this manner, an individual segment of the leadframe takes the form of a thin metallic strip with its particular geometric shape determined by the design. For most purposes, the length of a typical segment is considerably longer than its width.

In the European patent # 0 335 608 B1, issued 14 June 1995 (Abbott, "Leadframe with Reduced Corrosion"), a palladium-plated leadframe is introduced which is not subject to corrosion due to galvanic potential forces aiding the migration of the base metal ions to the top surface where they will form corrosion products. The patent describes a sequence of layers consisting of nickel (over the base metal), palladium/nickel alloy, nickel, and palladium (outermost). This technology has been widely accepted by the semiconductor industry.

After assembly on the leadframe, most ICs are encapsulated, commonly by plastic material in a molding process. It is essential that the molding compound, usually an epoxy-based thermoset compound, has good adhesion to the

leadframe and the device parts it encapsulates. Palladium, described above as the outermost layer of the leadframe, offers excellent adhesion to molding compounds.

Unfortunately, palladium is expensive; its price  
5 climbed in the last decade from about one third of the gold price to about 20 % higher than gold. Cost reduction pressures in semiconductor manufacturing have initiated efforts to reduce the thickness of the palladium layers employed to about one third of its previous thickness. At  
10 this thinness, palladium does not prevent oxidation of the underlying nickel which will inhibit its solderability. A method introduced in semiconductor manufacturing uses a thin layer of gold on the palladium surface to prevent oxidation. One related example is described in US Patent # 5,859,471,  
15 issued on Jan. 12, 1999 (Kuraishi et al., "Semiconductor Device having TAB Tape Leadframe with Reinforced Outer Leads").

In these methods, however, the entire surfaces of the leadframe are plated with gold. This practice severely  
20 inhibits the adhesion of the leadframe segments to molding compounds and risks delamination in thermomechanical stress testing. Furthermore, the plating of the complete leadframe with a thin gold layer makes it impossible to decide by visual inspection whether a leadframe has the gold surface  
25 or not. Such standard simple inspection, however, is highly desirable as manufacturing practice. Finally, the deposition of gold in unnecessary areas is counterproductive to cost saving efforts.

An urgent need has therefore arisen for a low-cost,  
30 reliable mass production method for a leadframe having reduced palladium layer thickness combined with solderability, bondability, adhesion capability to molding compounds, and visual inspection contrasts. The leadframe

and its method of fabrication should be flexible enough to be applied for different semiconductor product families and a wide spectrum of design and assembly variations, and should achieve improvements toward the goals of improved process yields and device reliability. Preferably, these innovations should be accomplished using the installed equipment base so that no investment in new manufacturing machines is needed.

## SUMMARY OF THE INVENTION

According to the present invention for a semiconductor integrated circuit (IC) leadframe, a plated layer of gold selectively covers areas of the leadframe intended for soldering, providing a visual distinction to those areas and optimizing solder attachment. While this layer of gold is very thin and thus barely adds to the leadframe cost, it enables substantial savings of underlying plated metals without diminishing the leadframe quality for wire bonding and for adhesion to molding compounds.

The present invention is related to high density ICs, especially those having high numbers of inputs/outputs, or contact pads, and also to devices in packages requiring surface mount in printed circuit board assembly. These ICs can be found in many semiconductor device families such as standard linear and logic products, digital signal processors, microprocessors, digital and analog devices, high frequency and high power devices, and both large and small area chip categories. The invention represents a significant cost reduction of the semiconductor packages, especially the plastic molded packages, compared to the conventional copper-based palladium-plated leadframes.

It is an aspect of the present invention to provide a technology for reducing the thickness of costly noble metal, especially palladium, layers while simultaneously improving the solderability the leadframe and maintaining its reliable adhesion to plastic molding compounds.

Another aspect of the invention is to reach these goals without the cost of equipment changes and new capital investment, by using the installed fabrication equipment base.

Another aspect of the present invention is to introduce a manufacturing quality check based on a simple, low-cost visual inspection. This check insures the selection of the correct leadframe and its appropriate preparation before releasing it into the assembly process flow.

These aspects have been achieved by the teachings of the invention concerning masking and deposition methods suitable for mass production. Various modifications of leadframe preparations have been successfully employed.

In the first embodiment of the invention, the frequently used layer sequence of first nickel, palladium-nickel alloy, second nickel and palladium is modified so that the palladium layer thickness is reduced across the entire leadframe and a thin layer of gold is selectively plated on lead segment areas intended for solder attachment, preventing the oxidation of the underlying nickel and thus preserving its solderability.

In the second embodiment of the invention, the first nickel layer and the palladium-nickel alloy layer are omitted. Again, solderability, bondability, adhesion to plastics, and corrosion insensitivity are demonstrated.

Leadframes prepared according to the invention can be successfully used in surface mount technologies based on bending the package lead segments.

The technical advances represented by the invention, as well as the aspects thereof, will become apparent from the following description of the preferred embodiments of the invention, when considered in conjunction with the accompanying drawings and the novel features set forth in the appended claims.



## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic cross sectional view of a portion of a leadframe made according to the first  
5 embodiment of the invention.

FIG. 2 is a schematic cross sectional view of a portion of a leadframe made according to the second embodiment of the invention.

FIG. 3 is a schematic and simplified cross sectional  
10 view of a package semiconductor device having a leadframe according to the invention, solder assembled on a substrate.

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## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention is related to the assembly of semiconductor ICs on leadframes and their final encapsulation, the sequential construction of these leadframes using deposited layers of various metals, and the process of fabricating these leadframes so that they offer quality-related visual inspection and reliable solder attachment to substrates.

The invention reduces the cost of leadframes while the leadframe functions are maximized. The invention best applies to any leadframe and any substrate used in semiconductor technology which exhibit the following design features: Usually, a chip pad for support of the IC chip surrounded by lead segments having an inner tip in proximity of the chip pad, and outer tips remote from the chip pad. The invention thus applies to semiconductor package types such as PDIPs, SOICs, QFPs, SSOPs, TQFPs, TSSOPs and TVSOPs.

For PDIPs, the gold spot is applied to both sides of the outer segments. For gull wing devices (see below FIG. 3), the gold spot is only required on the surface of the segment that faces the assembly board. For J-leaded devices, the gold is on the outside of the J-bend; it may also cover the edges of the segment.

The base metal of leadframes is typically copper or copper alloys. Other choices comprise iron-nickel alloys ("Alloy 42"), invar, or aluminum.

Leadframe segments have to satisfy five needs in semiconductor assembly:

- 1) Leadframes have to comprise outer segment tips for solder attachment to other parts;
- 2) leadframes have to comprise inner segment tips for bond attachments to wires;

3) leadframes have to comprise outer segments ductile for forming and bending the segments;

4) leadframe surfaces have to comprise adhesion to molding compounds; and

5) leadframe segments have to comprise insensitivity to corrosion.

According to the teachings of this invention, Need 1) is satisfied by selectively depositing a layer of gold where, and only where, a solder joint has to be made. This gold layer is plated over a layer of a noble metal, usually palladium, which is intentionally made thin. While at this thinness, the palladium would not prevent the oxidation of the underlying nickel, together with the thin gold layer such protection is provided and the solderability of the nickel guaranteed.

As stated above, the final form of the outer lead segments after bending determines where the gold is required.

The invention satisfies Need 2) by the choice of the noble metal layer employed to fulfill Need 1). For palladium, a thin layer is sufficient for reliable bonding wire attachment (stitch bonds, ball bonds, or wedge bonds).

The invention satisfies Need 3) by the selection of thickness and structure of the nickel layer employed to fulfill need 1). Thickness and deposition method of the nickel layer have to be selected such that the layer insures ductility and enables the bending and forming of the outer lead segments.

The invention satisfies Need 4) by the choice of the noble metal layer employed to fulfill need 1); a practical selection is palladium with its excellent adhesion to thermoset molding compounds and other encapsulation materials. From the standpoint of maximum adhesion, it is

an advantage that the invention avoids gold inside the finished package.

The invention satisfies Need 5) by the sequence of layers deposited over the copper base. The optimum corrosion insensitivity is achieved by the layer sequence described in FIG. 1.

In the embodiment of the invention in FIG. 1, the schematic cross section of a leadframe portion according to the invention is generally designated 100. The copper or copper alloy base sheet 101 has a preferred thickness in the range from 100 to 300  $\mu\text{m}$ ; thinner sheets are possible. The ductility in this thickness range provides the 5 to 15 % elongation needed in the segment bending and forming operation. The leadframe is stamped or etched from the starting metal sheet. The stamped or etched leadframe is first immersed in an alkaline preclean solution at 20 to 90  $^{\circ}\text{C}$  for few seconds up to 3 minutes. Oils, grease, soil, dirt and other contamination are thereby removed.

After rinsing, the leadframe is next immersed in an acid activation bath at room temperature for few seconds up to 5 minutes. The bath consists of a solution of sulfuric acid, hydrochlorid acid, or other acid solution, preferably at about 30 to 60 g/l concentration. This solution removes copper oxide and leaves the metallic copper oxide surface in an activated state, ready to accept the deposition of metallic nickel.

The nickel layer 102 is electroplated to a thickness in the range between about 50 and 150 nm. The next deposited layer 103 is an alloy between nickel and a noble metal selected from a group consisting of palladium, rhodium, gold silver, and platinum. The preferred choice is palladium, with 60 to 80 % palladium. The alloy layer is deposited by electroplating and between about 25 and 150 nm

thick; it should be coherent since its main purpose is corrosion protection.

The important layer 104 is electroplated nickel, deposited preferably for a thickness of about 0.5 to 3  $\mu\text{m}$ . This nickel layer has to be ductile in order to be malleable in the leadframe segment bending and forming process. Further, the nickel surface has to be wettable in the soldering process, so that solder alloys or conductive adhesives can be used successfully.

The overall thickness of the two nickel layers and the nickel alloy layer is in the range of about 650 to 4000 nm.

The next deposited layer of the embodiment in FIG. 1 is the layer 105, comprising an electroplated noble metal selected from a group consisting of palladium, rhodium, gold and silver. The preferred embodiment is palladium; however, if minimum interdiffusion with solder is desired, layer 105 may also consist of platinum. Since the cost of palladium has increased significantly in the last few years, it is important that the present invention reduces its thickness from the value it customarily had (about three times larger). According to the invention, layer 105 is preferably between about 10 and 30 nm thick, when palladium is chosen.

In this thickness range, palladium is suitable for all wire bonding attachments (stitch bonds, ball bonds, and wedge bonds) and retains its excellent adhesion to thermoplastic molding compounds - an attribute crucial for avoiding package delamination and progressive corrosion.

The outermost layer of the embodiment in FIG. 1 is layer 106, comprising selectively plated gold in the thickness range of about 2 to 5 nm. Its purpose is to prevent surface oxidation of the underlying layer 104

wherever solder joints are to be made. As FIG. 1 shows, a mask, covering portions of layer 105, allows the gold deposition beginning at a limit 106a so that the gold is spot-plated in the areas where solderablility is required.

5 In this thickness range, gold not only reliably provides good solderablilty, but also provides a visual distinction between the gold-plated areas and the adjacent palladium or nickel surfaces without gold deposition. This contrast between covered and uncovered areas can readily be  
10 seen by the unaided eye and is, therefore, well suited for automated visual inspection in manufacturing process control, contributing to product quality assurance.

There are several methods to selectively deposit metals from solution onto a continuous strip. For high  
15 volume production of leadframes, continuous strip or reel-to-reel plating is advantageous. The process steps of the preferred methods are as follows.

\*\* STEP AND REPEAT

- \* Leadframe material is stopped in selective  
20 plating head;
- \* rubber mask system clamps on material;
- \* plating solution is jetted at material;
- \* current is applied;
- \* current is shut off;
- 25 \* solution is shut off;
- \* head opens;
- \* material moves.

Advantages: Very sharp plating spot with excellent edge definition; very good spot location capability when used  
30 with index holes, pins and feedback vision system.

Disadvantages: Slow; material must stop during selective plating; expensive equipment to buy and maintain; timing issues; lots of moving parts.

\*\* WHEEL SYSTEM

- \* Material is moved over a large diameter wheel with apertures in it to allow solution flow to material;
- \* backing belt is used to hold material on wheel and mask backside of material;
- \* anode is stationary inside wheel.

Advantages: Fast, material never stops for selective plating; no timing issues; pumps, rectifiers, and drive system are on continuously; lower cost because less complicated mechanically.

Disadvantages: None for gold spot plating (poor edge shape, poor spot location, and bleedout are not critical issues).

In the embodiment of the invention shown in the schematic cross section of FIG. 2, the copper or copper alloy base of the leadframe is directly followed by the electroplated nickel layer 104; the additional nickel layer and the nickel/palladium alloy layer are omitted. The thickness range of nickel layer 104 is again about 0.5 to 3  $\mu\text{m}$ . According to the present invention, the electroplated noble metal layer 105 (for example, palladium) is only about 10 to 30 nm thick. The outermost layer is the thin, selectively plated gold layer 106 with a preferred thickness range from about 2 to 5 nm. As FIG. 2 shows, a mask allows the gold deposition to begin at limit 106a so that the gold is spot-plated in the areas where solderability is required.

In the schematic cross section of FIG. 3, the copper or copper alloy leadframe 301 of the invention is shown as applied in the assembly of a semiconductor package generally designated 300. Leadframe 301 has a chip mount pad 302 onto which an IC chip 303 is attached using adhesive material 304 (typically an epoxy or polyimide which has to undergo polymerization). Leadframe 301 further has a plurality of

lead segments 305. These lead segments have a first end 305a near the chip mount pad 302 and their second end 305b remote from mount pad 302.

As shown in FIG. 3 schematically, leadframe 305  
5 comprises base 306 made of copper or copper alloy. On the surface of this copper is a sequence of layers, described in detail in FIG. 1. Closest to the copper is a first layer 307 of nickel. This layer is followed by an alloy layer 308 made of nickel and a noble metal, preferably palladium, and  
10 a second layer 309 of nickel. The top layer inside the package and on some portions of lead segments 305 is layer 310, made of a noble metal, preferably palladium.

As described in conjunction with FIG. 1, this sequence of layers provides reliable protection against  
15 corrosion, reliable adhesion to the plastic encapsulation compound, and reliable wire bonding for connecting the chip contact pads to the leadframe segments. In FIG. 3, bonding wires 311 have stitches 312 welded to the palladium surface 310 of leadframe segments 305. The bonding wires are  
20 selected from a group consisting of gold, copper, aluminum, and alloys thereof. Any of these metals provide reliable welds to the layered leadframes of the invention.

As shown in FIG. 3, the second ends 305b of segments 305 are suitable for bending and forming due to the  
25 ductility of the copper base and the electroplated nickel layer. Using this malleable characteristic, segments 305 may be formed in any shape required for surface mounting or any other technique of board attach of the semiconductor devices. The bending of the segments does not diminish the  
30 corrosion protection of the second segment ends 305b. For example, FIG. 3 indicates a so-called "gull wing shape" of segments 305. This shape is widely used for IC packages in



the so-called "small outline" configuration, as illustrated in FIG. 3.

Outermost layer 313 in FIG. 3 is the spot-plated thin gold layer of the present invention. This gold layer covers the area of the outer segment ends 305b where the solder joints are made. Due to border line 313a, the gold can be distinguished from the palladium and nickel surface near the plastic outline. In an embodiment different from FIG. 3, the gold of gull-wing devices covers only the surface of the segments that face the assembly board; in this case, the gold can also be distinguished from the palladium surface when compared to the reverse side of the segment.

The gold spot-plated copper leadframe of the invention provides for easy and reliable solder attachment to boards or other parts of the formed leadframe segments. In FIG. 3, solder attach material 314 comprises materials selected from a group consisting of tin/lead mixture, tin/indium, tin/silver, tin/bismuth, and conductive adhesive compounds. When palladium is selected as the metal of layer 310, it may be dissolved (not shown in FIG. 3) into the solder material during the attachment process so that direct solder wetting to the nickel layer 309 is achieved.

In FIG. 3, molding compound 315 encapsulates the mounted chip 303, bonding wires 311 and the first ends 305a of the lead segments 305. The second, remote ends 305b of the segments are not included in the molded package; they remain exposed for solder attachment. Typically, the encapsulation material 315 is selected from a group consisting of epoxy-based molding compounds suitable for adhesion to layer 310 of the leadframe. For palladium, excellent adhesion characteristics to molding compounds can be achieved, preventing package delamination, moisture ingress and corrosion.

While this invention has been described in reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative 5 embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. As an example, the material of the semiconductor chip may comprise silicon, silicon germanium, gallium arsenide, or any other semiconductor 10 material used in manufacturing. As another example, the design, cover area and fabrication method of the gold layer may be modified to suit specific leadframe or substrate needs. It is therefore intended that the appended claims encompass any such modifications or embodiments.

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WE CLAIM:

1. A leadframe for use with integrated circuit chips comprising:

5       a plated layer of gold selectively covering areas of  
      said leadframe intended for solder attachment; and  
      said gold layer providing a visual distinction  
      to said areas.

- 10   2. A leadframe for use with integrated circuit chips,  
     having a chip mount pad and a plurality of lead  
     segments, comprising:

15       a leadframe base made of copper or copper alloy;  
      a first layer of nickel deposited on said copper or  
      copper alloy;  
      a layer of an alloy of nickel and palladium on said  
      first nickel layer;  
      a second layer of nickel on said alloy layer, said  
      second nickel layer deposited to be suitable for  
      bending of said lead segments, wire bonding, and  
20       solder attachment;  
      a layer of palladium, said palladium layer deposited  
      to be suitable for protecting the nickel surface  
      for wire bonding and solderability, and for  
      adhesion to molding compound; and  
25       a layer of gold selectively covering areas of said  
      lead segments intended for solder attachment, said  
      layer of gold providing a visual distinction to  
      said areas and having a thickness to optimize  
      solder attachment.

- 30   3. The leadframe according to Claim 2 wherein said gold  
     layer has a thickness in the range from 2 to 5 nm.
4. The leadframe according to Claim 2 wherein said first  
     nickel layer has a thickness in the range from 50 to 150

nm.

5. The leadframe according to Claim 2 wherein said alloy layer has a thickness in the range from 50 to 150 nm.
6. The leadframe according to Claim 2 wherein said second nickel layer has a thickness in the range from 1000 to 3000 nm.
7. The leadframe according to Claim 2 wherein said palladium layer has a thickness in the range from 25 to 75 nm.
8. The leadframe according to Claim 2 wherein said copper or copper alloy base has a thickness between about 100 and 250  $\mu\text{m}$ .
9. The leadframe according to Claim 2 wherein said solder attachment comprises solder materials selected from a group consisting of tin/lead, tin/indium, tin/silver, tin/bismuth and conductive adhesive compounds.
10. The leadframe according to Claim 1 wherein said leadframe comprises an iron-nickel alloy or invar base, selectively plated with gold.
11. A semiconductor device comprising:
  - a leadframe comprising a chip mount pad for an integrated circuit chip and a plurality of lead segments having their first end near said mount pad and their second end remote from said mount pad;
  - said leadframe having a first surface layer of nickel, a layer of an alloy of nickel and palladium, a second layer of nickel, and a layer of palladium;
  - said leadframe further having an outermost layer of gold selectively covering said second ends of said lead segments in a thickness suitable to optimize solder attachment;

an integrated circuit chip attached to said mount pad;

bonding wires interconnecting said chip and said first ends of said lead segments;

5        encapsulation material surrounding said chip, bonding wires and said first ends of said lead segments, whereby the adhesion between said encapsulation material and said surrounded parts is maximized; and

10        said encapsulation material leaving said second ends of said lead segments exposed, whereby the solder attachment to said gold layer is maximized.

12. The device according to Claim 11 wherein said bonding wires are selected from a group consisting of gold, copper, aluminum and alloys thereof.

13. The device according to Claim 11 wherein the bonding wire contacts to said first ends of said lead segments comprise welds made by ball bonds, stitch bonds, or wedge bonds.

14. The device according to Claim 11 wherein said encapsulation material is selected from a group consisting of epoxy-based molding compounds suitable for adhesion to said leadframe.

15. The device according to Claim 11 further comprising lead segments having said second ends bent, whereby said segments obtain a form suitable for solder attachment.

16. A method for fabricating a leadframe comprising a chip mount pad and a plurality of lead segments having their first end near said mount pad and their second end remote from said mount pad, comprising the steps of:  
selectively masking said chip pad and said first segment ends, thereby leaving said second segment ends exposed; and

plating a layer of gold on said exposed segment ends  
in a thickness suitable to optimize solder  
attachment, thereby creating a visual distinction  
between the gold-plated and unplated leadframe  
areas.

17. A method for fabricating a leadframe comprising the  
steps of:

providing a copper leadframe having a mount pad for  
an integrated circuit chip and a plurality of lead  
segments having their first end near said mount  
pad and their second end remote from said mount  
pad;

cleaning said leadframe in alkaline soak cleaning and  
alkaline electrocleaning;

activating said leadframe by immersing said leadframe  
into an acid solution, thereby dissolving any  
copper oxide;

immersing said leadframe into an electrolytic nickel  
plating solution and depositing a first layer of  
nickel onto said copper;

electroplating a layer comprising an alloy of nickel  
and palladium;

electroplating a second layer of nickel, thereby  
adapting said lead segments for mechanical  
bending;

electroplating a layer of palladium;

selectively masking said chip pad and said first  
segment ends, thereby leaving said second segment  
ends exposed; and

plating a layer of gold on said exposed segment ends  
in a thickness suitable to optimize solder  
attachment, thereby creating a visual distinction  
between the gold-plated and unplated leadframe

areas.

18. The method according to Claim 17 wherein said gold plating is performed electrolytically or electrolessly.

19. The method according to Claim 17 wherein said masked  
5 parts of said leadframe comprise the leadframe areas to be encapsulated by molding compound.

20. The method according to Claim 17 wherein the process steps are executed in sequence without time delays, yet including intermediate rinsing steps.

10 21. The method according to Claim 17 wherein said acid solution may be sulfuric acid, hydrochloric acid or any other acid.

22. A method for fabricating a leadframe comprising the steps of:

15 providing a copper leadframe having a mount pad for an integrated circuit chip and a plurality of lead segments having their first end near said mount pad and their second end remote from said mount pad;

20 cleaning said leadframe in alkaline soak cleaning and alkaline electrocleaning;  
activating said leadframe by immersing said leadframe into an acid solution, thereby dissolving any copper oxide;

25 electroplating a layer of nickel, thereby adapting said lead segments for mechanical bending;  
electroplating a layer of palladium;  
selectively masking said chip pad and said first segment ends, thereby leaving said second segment  
30 ends exposed; and

plating a layer of gold on said exposed segment ends in a thickness suitable to optimize solder attachment, thereby creating a visual distinction

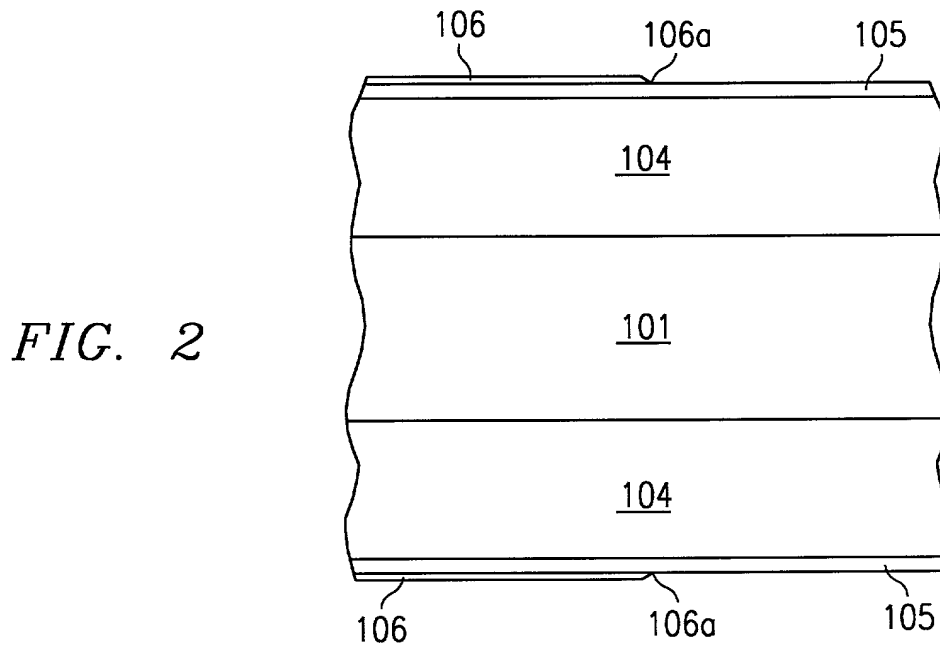
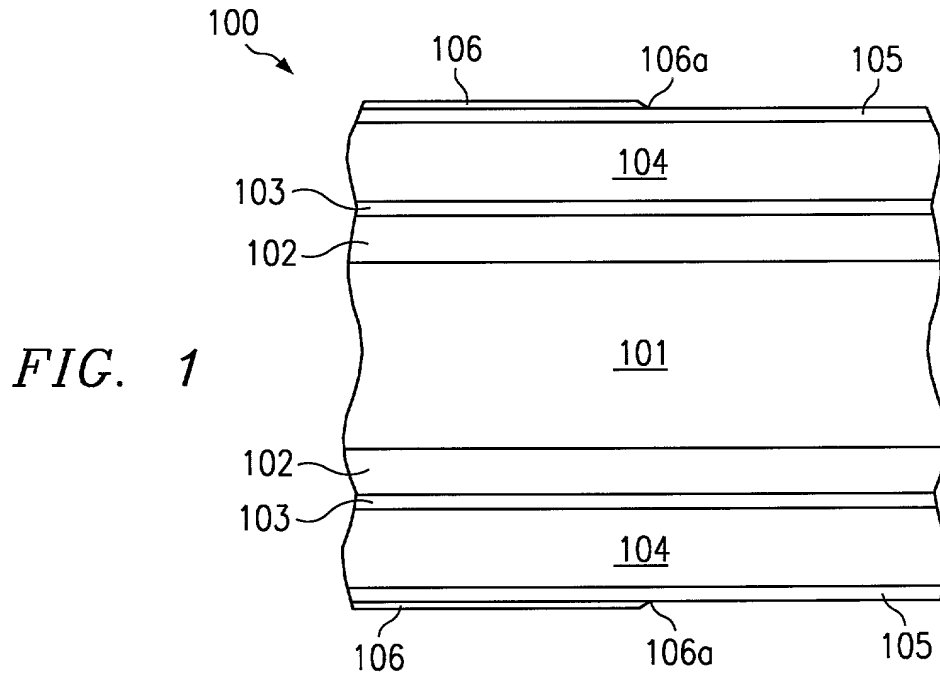
between the gold-plated and unplated leadframe areas.

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	1997-1998	1998-1999	1999-2000	2000-2001	2001-2002	2002-2003	2003-2004	2004-2005	2005-2006	2006-2007	2007-2008	2008-2009	2009-2010	2010-2011	2011-2012	2012-2013	2013-2014	2014-2015	2015-2016	2016-2017	2017-2018	2018-2019	2019-2020	2020-2021	2021-2022	2022-2023	2023-2024	2024-2025	2025-2026	2026-2027	2027-2028	2028-2029	2029-2030	2030-2031	2031-2032	2032-2033	2033-2034	2034-2035	2035-2036	2036-2037	2037-2038	2038-2039	2039-2040	2040-2041	2041-2042	2042-2043	2043-2044	2044-2045	2045-2046	2046-2047	2047-2048	2048-2049	2049-2050	2050-2051	2051-2052	2052-2053	2053-2054	2054-2055	2055-2056	2056-2057	2057-2058	2058-2059	2059-2060	2060-2061	2061-2062	2062-2063	2063-2064	2064-2065	2065-2066	2066-2067	2067-2068	2068-2069	2069-2070	2070-2071	2071-2072	2072-2073	2073-2074	2074-2075	2075-2076	2076-2077	2077-2078	2078-2079	2079-2080	2080-2081	2081-2082	2082-2083	2083-2084	2084-2085	2085-2086	2086-2087	2087-2088	2088-2089	2089-2090	2090-2091	2091-2092	2092-2093	2093-2094	2094-2095	2095-2096	2096-2097	2097-2098	2098-2099	2099-2100	2100-2101	2101-2102	2102-2103	2103-2104	2104-2105	2105-2106	2106-2107	2107-2108	2108-2109	2109-2110	2110-2111	2111-2112	2112-2113	2113-2114	2114-2115	2115-2116	2116-2117	2117-2118	2118-2119	2119-2120	2120-2121	2121-2122	2122-2123	2123-2124	2124-2125	2125-2126	2126-2127	2127-2128	2128-2129	2129-2130	2130-2131	2131-2132	2132-2133	2133-2134	2134-2135	2135-2136	2136-2137	2137-2138	2138-2139	2139-2140	2140-2141	2141-2142	2142-2143	2143-2144	2144-2145	2145-2146	2146-2147	2147-2148	2148-2149	2149-2150	2150-2151	2151-2152	2152-2153	2153-2154	2154-2155	2155-2156	2156-2157	2157-2158	2158-2159	2159-2160	2160-2161	2161-2162	2162-2163	2163-2164	2164-2165	2165-2166	2166-2167	2167-2168	2168-2169	2169-2170	2170-2171	2171-2172	2172-2173	2173-2174	2174-2175	2175-2176	2176-2177	2177-2178	2178-2179	2179-2180	2180-2181	2181-2182	2182-2183	2183-2184	2184-2185	2185-2186	2186-2187	2187-2188	2188-2189	2189-2190	2190-2191	2191-2192	2192-2193	2193-2194	2194-2195	2195-2196	2196-2197	2197-2198	2198-2199	2199-2200	2200-2201	2201-2202	2202-2203	2203-2204	2204-2205	2205-2206	2206-2207	2207-2208	2208-2209	2209-2210	2210-2211	2211-2212	2212-2213	2213-2214	2214-2215	2215-2216	2216-2217	2217-2218	2218-2219	2219-2220	2220-2221	2221-2222	2222-2223	2223-2224	2224-2225	2225-2226	2226-2227	2227-2228	2228-2229	2229-2230	2230-2231	2231-2232	2232-2233	2233-2234	2234-2235	2235-2236	2236-2237	2237-2238	2238-2239	2239-2240	2240-2241	2241-2242	2242-2243	2243-2244	2244-2245	2245-2246	2246-2247	2247-2248	2248-2249	2249-2250	2250-2251	2251-2252	2252-2253	2253-2254	2254-2255	2255-2256	2256-2257	2257-2258	2258-2259	2259-2260	2260-2261	2261-2262	2262-2263	2263-2264	2264-2265	2265-2266	2266-2267	2267-2268	2268-2269	2269-2270	2270-2271	2271-2272	2272-2273	2273-2274	2274-2275	2275-2276	2276-2277	2277-2278	2278-2279	2279-2280	2280-2281	2281-2282	2282-2283	2283-2284	2284-2285	2285-2286	2286-2287	2287-2288	2288
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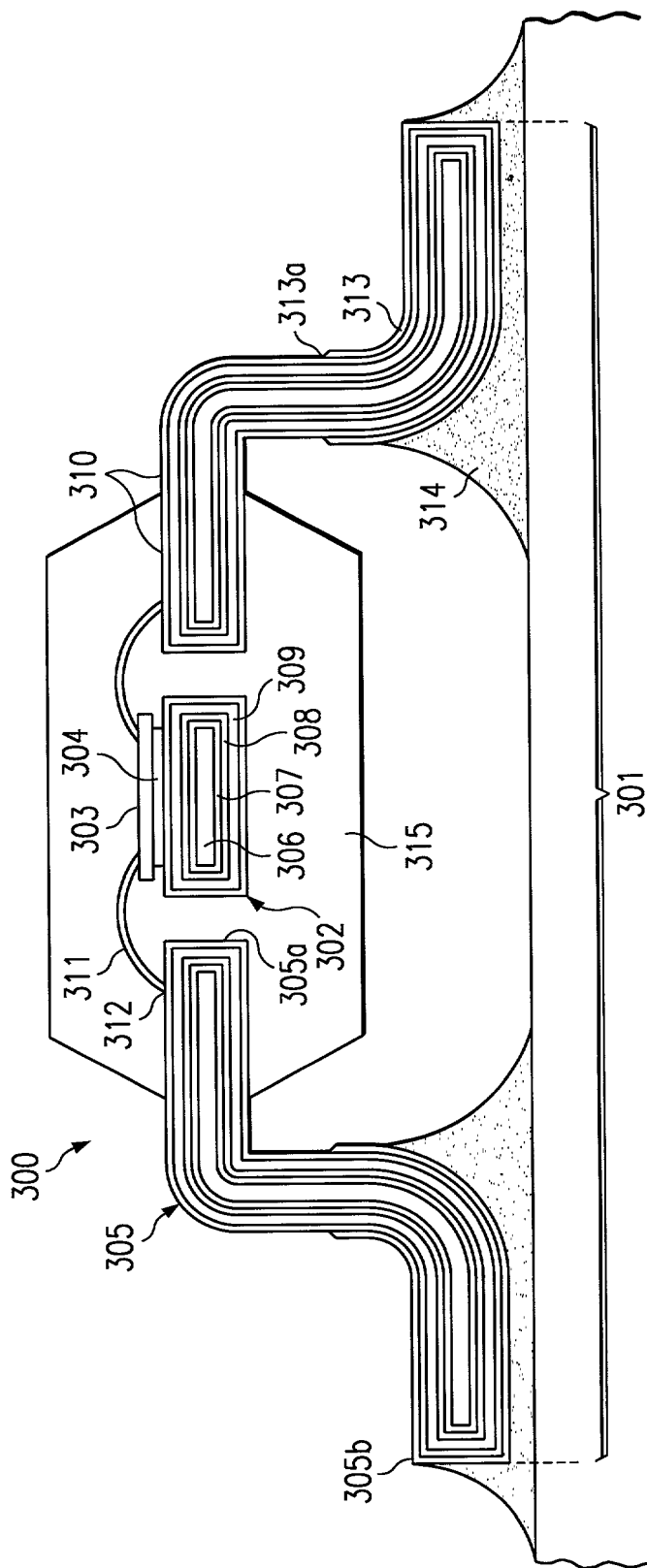
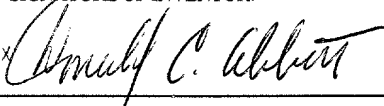
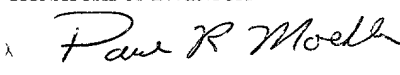


FIG. 3

# **APPLICATION FOR UNITED STATES PATENT DECLARATION AND POWER OF ATTORNEY**

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56;

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION:		
Gold Spot Plated Leadframes for Semiconductor Devices and Method of Fabrication		
POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH Richard L. Donaldson, #25,673; Jay M. Cantor, #19,906; William B.Kempler, #28,228; Lawrence J.Bassuk, #29,043 and Gary C.Honeycutt, #20,250		
SEND CORRESPONDENCE TO: Gary C. Honeycutt Texas Instruments Incorporated P.O. Box 655474, MS 3999 Dallas, TX 75265		DIRECT TELEPHONE CALLS TO:  Gary C. Honeycutt (972) 238-7160
NAME OF INVENTOR: (1)  Donald C. Abbott	NAME OF INVENTOR: (2)  Paul R. Moehle	NAME OF INVENTOR: (3)  N/A
RESIDENCE & POST OFFICE ADDRESS:  P.O. Box 357 4 Fernandes Circle Norton, Massachusetts 02766	RESIDENCE & POST OFFICE ADDRESS:  221 Walker Street Seekonk, Massachusetts 02771	RESIDENCE & POST OFFICE ADDRESS:
COUNTRY OF CITIZENSHIP:  United States	COUNTRY OF CITIZENSHIP:  United States	COUNTRY OF CITIZENSHIP:
SIGNATURE OF INVENTOR: 	SIGNATURE OF INVENTOR: 	SIGNATURE OF INVENTOR:
DATE: X March 22, 1999	DATE: X March 22, 1999	DATE: